|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  |  | R2 |  | R1 | R3 |
| R Format | opcode | Rm | Shamt | Rn | Rd |
| 11 bits | 5 bits | 6 bits | 5 bits | 5 bits |

SUB Rd = Rn - Rm SUB R3, R1, R2

ADD Rd = Rm + Rn

AND Rd = Rm & Rn

ORR Rd = Rm | Rn

EOR Rd = Rm ^ Rn

LSL Rd = Rn << Shamt

ASR Rd = Rn >> Shamt pad with sign bit <- PYTHON SYNTAX ISSUE!!!!!!

LSR Rd = Rn shifted Shamt right pad with zeros

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| D Format | opcode | address | op2 | Rn | Rt |
| 11 bits | 9 bits | 2 bits | 5 bits | 5 bits |

# Add the offset in address register to Rn to get target address.

# Either load value in Rt into address

11111000000 000000001 00 00100 00010 108 STUR R2, [R4, #1]

STUR Rt(R2) = [Rn + address]

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| I Format | opcode | immediate | Rn | Rd |
| 10 bits | 12 bits | 5 bits | 5 bits |

immediate is unsigned int

ADDI Rd = Rn + immediate ADDI R3, R1, #Immed

|  |  |  |
| --- | --- | --- |
| B Format | opcode | offset (w) |
| 6 bits | 26 bits |

offset is signed value - use two's compliment

|  |  |  |  |
| --- | --- | --- | --- |
| CB Format | opcode | offset (w) | conditional |
| 8 bits | 19 bits | 5 bits |

offset is signed value - use two's compliment

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| IM Format | opcode | shift code | field | Rd |
| 9 bits | 2 bits | 16 bits | 5 bits |

field is unsigned value - is 16 bit pattern